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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,493	12/11/2003	Yew Wee Cheong	42P17612	1630

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EXAMINER	
MCNALLY, DANIEL	
ART UNIT	**PAPER NUMBER**
1733	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/734,493	CHEONG ET AL.	
	Examiner	Art Unit	
	Daniel McNally	1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11,12,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,12,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a response to the amendment filed November 30, 2006.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 4-6 and 8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Clam 1 was amended to include the phrase, "without applying adhesive tape in addition to the protective layer." The specification of the invention does not include the negative limitation recited above. The applicant is recommended to positively recite the limitation in a manner that is supported by the specification. Claims 4-6 and 8 are dependent upon claim 1.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Applicant has provided evidence in this file showing that the invention was owned by, or subject to an obligation of assignment to, the same entity as Kumamoto [US-2003/0001283] at the time this invention was made, or was subject to a joint research agreement at the time this invention was made. However, reference Kumamoto [US-2003/0001283] additionally qualifies as prior art under another subsection of 35 U.S.C. 102, namely 102(a) and therefore, is not disqualified as prior art under 35 U.S.C. 103(c).

Applicant may overcome the applied art either by a showing under 37 CFR 1.132 that the invention disclosed therein was derived from the invention of this application, and is therefore, not the invention "by another," or by antedating the applied art under 37 CFR 1.131.

6. Claims 1, 4, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamoto [US-2003/0001283] as applied in paragraph 7 of the Office action dated 8/21/2006 in view of Walsh [US3475867] (newly cited).

Kumamoto discloses a method of producing a chip assembly. Kumamoto discloses the application of a coating 550' to a wafer 110, covering bumps 130 or "connection structures" (paragraph 0035). Note the discloser of a backgrinding process 350 (paragraph 0039), and the dicing of the wafer 800 into dice (paragraph 0042). Kumamoto also discloses connecting a die 800' to a substrate 960 (paragraph 0043), so the coating is between the die and the substrate as seen in Figure 13. Kumamoto discloses applying an adhesive tape layer to the wafer before the grinding process,

removing the tape after the grinding process and does not satisfy the negative limitation of claim 1.

Walsh discloses a method of processing semiconductors. The method comprises spreading a wax coating on a carrier plate and depositing semiconductor wafers into the wax to mount the wafers on the carrier plate (column 7, lines 41-50). The mounted wafers then have a portion of the back surface of the wafer removed in a lapping machine (column 8, lines 35-55). After the wafers reach a desired thickness and are polished, the wafers are removed from the wax and carrier plate.

It would have been obvious to one of ordinary skill in the art at the time of invention to replace the adhesive tape of Kumamoto with wax to hold the wafer on a carrier plate during the back grind process as taught by Walsh in order to reduce the waste of the adhesive tape because the wax can be recycled and reused while the adhesive tape is good for only a single application.

With respect to claim 4, Kumamoto discloses a solder-bumped wafer (paragraph 0022) comprising solder bumps 130 or "balls" as seen in Figure 1.

With respect to claim 5, Kumamoto discloses the application of heat to connect bumps 130 and lands 970 by solder flow (paragraph 0043).

Kumamoto discloses a method of dicing a wafer into dice as discussed with regard to claim 1. With respect to claim 8, Kumamoto also discloses a single die 800' being flipped together with its coating (paragraph 0042). Figure 9 shows the die and coating remains in contact.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamoto in view of Walsh as applied in paragraph 6 above further in view of Nguyen et al. [US6352881].

Kumamoto, as modified, discloses a method of producing a chip assembly. The applicant is referred to paragraph 6 above for a detailed discussion of Kumamoto, as modified. Note Kumamoto discloses the coating 550' as a thermoset polymer in (paragraph 0036). Epoxy is a thermoset polymer but Kumamoto does not specifically disclose the use and partial curing of epoxy, as recited in claim 6.

Nguyen disclose a method of producing a flip chip assembly comprising a step of applying a layer of underfill adhesive 110 to a wafer 100 (column 3, lines 13-19). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47), and that it is partially cured after application.

It would have been obvious to one of ordinary skill in the art at the time of invention to use an epoxy based material in the coating of Kumamoto, as modified, and to partially cure the coating after application as taught by Nguyen in order to have an easy to handle chip with an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip.

8. Claims 2, 3, 7, 9, 11, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamoto in view of Nguyen et al. for the same reasons as expressed in paragraph 9 of the Office action dated 8/21/2006.

Claims 2, 3 and 18 are rejected for the same reasons as expressed in paragraph 9 of the Office action dated 8/21/2006.

With respect to claim 7, in addition to the reasons expressed in paragraph 9 of the Office action dated 8/21/2006, Kumamoto further discloses a solder-bumped wafer (paragraph 0022) comprising solder bumps 130 or "balls" as seen in Figure 1. Kumamoto also discloses the application of heat to connect bumps 130 and lands 970 by solder flow (paragraph 0043).

With respect to claim 9, Kumamoto discloses a method of producing a chip assembly. See the detailed discussion of Kumamoto as modified by Nguyen as applied in claims 2, 3 and 7 above.

With respect to claim 11, because the coating is not removed from the die, the coating and die remain in contact while they are separated into single pieces from the wafer.

With respect to claim 12, Kumamoto also discloses connecting a die 800' to a substrate 960 (paragraph 0043), so the coating is between the die and the substrate as seen in Figure 13.

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamoto in view of Nguyen et al. and further in view of White [US-5535526] as applied in paragraph 10 of the Office action dated 8/21/2006.

10. Claims 1, 4-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh [US6338980] (of record, newly cited) in view of Nguyen and Walsh.

With respect to claim 1, Satoh discloses a method of forming a plurality of chips. The method comprises applying a protective resin to the active face of an IC wafer covering projected electrodes, grinding the inactive face of the IC wafer and dicing the wafer into a plurality of chips (column 3, lines 28-51). Satoh discloses applying an adhesive tape layer to the wafer before the grinding process, removing the tape after the grinding process and does not satisfy the negative limitation of claim 1. Satoh also does not disclose attaching the chip to a substrate as recited in claim 1.

Walsh discloses a method of processing semiconductors. The method comprises spreading a wax coating on a carrier plate and depositing semiconductor wafers into the wax to mount the wafers on the carrier plate (column 7, lines 41-50). The mounted wafers then have a portion of the back surface of the wafer removed in a lapping machine (column 8, lines 35-55). After the wafers reach a desired thickness and are polished, the wafers are removed from the wax and carrier plate.

Nguyen discloses a method of producing a flip chip assembly. Nguyen discloses aligning and mounting the flip chip onto a substrate so that the underfill is between the flip chip and the substrate (column 4, lines 30-38).

It would have been obvious to one of ordinary skill in the art at the time of invention to replace the adhesive tape of Satoh with wax to hold the wafer on a carrier plate during the back grind process as taught by Walsh in order to reduce the waste of the adhesive tape because the wax can be recycled and reused while the adhesive tape

is good for only a single application and mount the chip on a substrate as taught by Nguyen in order to enable the chip to communicate with outside circuitry coupled to the substrate.

With respect to claim 4, Satoh discloses the projected electrodes as solder bumps (column 5, lines 41-46).

With respect to claim 5, Nguyen discloses applying heat to flow the solder balls (column 4, lines 30-38).

With respect to claim 6 Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47), and that it is partially cured after application.

With respect to claim 8, Satoh discloses in Figures 1D and 1E the step of dicing the wafer into a plurality of chips. The figure shows as the wafer is diced the protective coating is also cut into separate sections.

11. Claims 2, 3, 7, 9, 11, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh [US6338980] in view of Nguyen.

With respect to claim 2, Satoh discloses a method of forming a plurality of chips. The method comprises applying a protective resin to the active face of an IC wafer covering projected electrodes, grinding the inactive face of the IC wafer and dicing the wafer into a plurality of chips (column 3, lines 28-51). Satoh does not disclose the protective resin as an epoxy or attaching the chip to a substrate.

Nguyen discloses a method of producing a flip chip assembly. Nguyen discloses aligning and mounting the flip chip onto a substrate so that the underfill is between the

flip chip and the substrate (column 4, lines 30-38). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47),

It would have been obvious to one of ordinary skill in the art at the time of invention mount the chip of Satoh on a substrate as taught by Nguyen in order to enable the chip to communicate with outside circuitry coupled to the substrate and to use an epoxy based material as taught by Nguyen in order to have an easy to handle chip with an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip.

With respect to claim 3, Nguyen discloses a soft or pre-cure operation is performed to partially cure the underfill adhesive (column 4, lines 16-28).

With respect to claim 7, Satoh discloses the projected electrodes as solder bumps (column 5, lines 41-46). Nguyen discloses applying heat to flow the solder balls (column 4, lines 30-38). Nguyen teaches the application of heat causes the solder balls 108 to flow and finally cure the underfill adhesive.

With respect to claim 9, Satoh discloses a method of forming a plurality of chips. The method comprises applying a protective resin to the active face of an IC wafer covering projected electrodes, grinding the inactive face of the IC wafer and dicing the wafer into a plurality of chips (column 3, lines 28-51). Satoh does not disclose the protective resin as an epoxy, partially curing the epoxy or finally curing the epoxy.

Nguyen discloses a method of producing a flip chip assembly. Nguyen discloses aligning and mounting the flip chip onto a substrate so that the underfill is between the flip chip and the substrate (column 4, lines 30-38). Nguyen teaches that the underfill can

be epoxy based (column 4, lines 40-47). Nguyen discloses a soft or pre-cure operation is performed to partially cure the underfill adhesive (column 4, lines 16-28). Nguyen discloses applying heat to flow the solder balls to join the chip to the substrate (column 4, lines 30-38). Nguyen teaches the application of heat causes the solder balls 108 to flow and finally cure the underfill adhesive.

It would have been obvious to one of ordinary skill in the art at the time of invention to use an epoxy based material as the resin of Satoh as taught by Nguyen in order to have an easy to handle chip with an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip, and to partially cure the epoxy as taught by Nguyen so that the epoxy remains in place on the chip and to finally cure the epoxy by applying heat as taught by Nguyen in order to make the epoxy layer harder and more protective.

With respect to claim 11, Satoh discloses in Figures 1D and 1E the step of dicing the wafer into a plurality of chips. The figure shows as the wafer is diced the protective coating is also cut into separate sections and that the protective layer remains in contact with the chip.

With respect to claim 12, Nguyen discloses attaching the chip to a substrate. Figure 1(g) shows the substrate and chip assembly where the underfill/protective layer is between the chip and substrate.

With respect to claim 18, Satoh discloses a method of forming a plurality of chips. The method comprises applying a protective resin to the active face of an IC wafer covering projected electrodes, grinding the inactive face of the IC wafer and dicing the

wafer into a plurality of chips (column 3, lines 28-51). Satoh does not disclose the protective resin as an epoxy, partially curing the epoxy or attaching the chip to a substrate by using heat, which fully cures the protective layer.

Nguyen disclose a method of producing a flip chip assembly comprising a step of applying a layer of underfill adhesive 110 to a wafer 100 and around solder balls 108 (column 3, lines 13-19). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47), that it is partially cured after application and the heat applied to melt the solder balls 108 will cure the underfill adhesive.

It would have been obvious to one of ordinary skill in the art at the time of invention to use an epoxy based material in Satoh's coating, to partially cure the coating after application and to finish curing the coating as taught by Nguyen in order to have an easy to handle chip with an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip.

12. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh in view of Nguyen et al. as applied in paragraph 11 above and further in view of White [US-5535526].

Satoh, as modified, discloses a method of producing a chip assembly as discussed with regard to claim 18, in paragraph 11 above. The references do not disclose coupling the substrate to a circuit board. White teaches a method of mounting a substrate 404 on a circuit board 416 (column 7, lines 24-45). White also discloses a flip chip 402 connected to the substrate by solder joints 406 and an encapsulant 408 or

"protective layer" between the flip chip and substrate. It would have been obvious to one of ordinary skill in the art at the time of invention to connect chip assembly of the references used in paragraph 11 to a circuit board as taught by White in order to expand the capabilities of the chip.

Response to Arguments

13. The amendment to the specification is noted and the objection is withdrawn.

14. Applicant's arguments with respect to claims 1-9, 11, 12, 18 and 19 have been considered but are moot in view of the new ground(s) of rejection.

Using wax in place of an adhesive tape to create a bond prior to back grinding the substrate would have been obvious in light of Walsh (newly cited).

15. Applicant's arguments, see page 7, filed 11/30/2006, with respect to the rejection(s) of claim(s) 1,4,5,8,9,11-13,15 and 16 under 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Walsh.

The applicant argued that the amendment to claim 1 over came the 102(e) rejection, which was withdrawn. The applicant also argued that Kumamoto could not be used in a 103(a) rejection because the reference was only applicable under 102(e). Kumamoto is also applicable as prior art under 102(a) therefore it is still applicable under 103(a) and the 103(a) rejections citing Kumamoto have been maintained.

The applicant does not argue the application of Nguyen. It is therefore asserted that the applicant agrees with the Office's interpretation of the reference for what it was applied for and the reasoning as to why the teachings of the reference would have been combined.

The applicant does not argue the application of White. It is therefore asserted that the applicant agrees with the Office's interpretation of the reference for what it was applied for and the reasoning as to why the teachings of the reference would have been combined.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel McNally whose telephone number is (571) 272-2685. The examiner can normally be reached on Monday - Friday 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel McNally
Examiner
Art Unit 1733

JEFF H. AFTERGUT
PRIMARY EXAMINER
GROUP 1300

dpm
January 9, 2007